CLAIMS

1. An integrated device, comprising: a substrate wherein a buried layer and an epitaxial region have been formed, and an isolation structure adapted to define a plurality of isolation wells for integrating the components of the integrated device therein, said isolation structure comprises plural dielectrically insulated trenches filled with a conductive material to form a plurality of contact regions to buried regions of the device, said buried regions including, in particular, the substrate and buried layer.

2. The integrated device of claim 1 wherein said dielectric trenches are formed at the edges of the isolation wells in contact with said buried layer.

3. The integrated device of claim 1 wherein said dielectric trenches are formed in intervening areas between adjacent isolation wells in contact with said substrate.

4. The integrated device of claim 2 wherein each isolation well comprises, located at each of its edges, a plurality of trenches in contact with said buried layer.

5. The integrated device of claim 3 wherein each intervening area between adjacent isolation wells includes a plurality of trenches in contact with said substrate.

6. The integrated device of claim 1 wherein said plurality of trenches comprise dielectric regions surrounding the contact regions.

7. The integrated device of claim 1, comprising active or parasitic components integrated in intervening regions between each of the plurality of trenches.

8. The integrated device of claim 1 wherein said isolation structure contacts buried regions of high- or low-voltage active components of the integrated device.

9. A process for fabricating an integrated device with an isolation structure, comprising:

providing a substrate, doped with a first dopant type;

masking the substrate, implanting and diffusing dopant of a second type to form buried layers; and

growing an epitaxial region doped with said dopant of the second type;

comprising:

forming a plurality of trenches; and

filling said trenches with a conductive material to form a plurality of contact regions to the buried layers of the device.

10. The process for fabricating an integrated device with an isolation structure of claim 9 wherein forming a plurality of trenches comprises:

oxidizing the epitaxial region and depositing a layer of silicon nitride;

depositing photoresist, exposing and developing the photoresist, sequentially etching the nitride and thermal oxide away from regions uncovered with the photoresist, and removing the photoresist;

dry etching the silicon underneath, as far down as said buried regions; and

oxidizing the trench sidewalls.

11. The process for fabricating an integrated device with an isolation structure of claim 10 wherein forming a plurality of trenches further comprises:

dry etching to pierce the bottoms of the oxidized trenches.

12. The process for fabricating an integrated device with an isolation structure of claim 11, further comprising a channeling implant step, carried out after dry etching.

13. The process for fabricating an integrated device with an isolation structure according to claim 9 wherein said step of filling the trenches with a conductive material comprises:

depositing said conductive material onto the entire surface such that the surface is contacting said buried layers.

14. The process for fabricating an integrated device with an isolation structure of claim 13 wherein said conductive material comprises polysilicon, and said depositing said conductive material is followed by polysilicon doping to lower the polysilicon resistivity and form resistive contacts.

15. The process for fabricating an integrated device with an isolation structure of claim 14 wherein said doping said polysilicon includes a selective masking and implanting sub-step, directly following depositing the polysilicon.

16. The process for fabricating an integrated device with an isolation structure of claim 14, comprising:

implanting said first-type dopant in the entire surface directly after depositing the polysilicon; and

masking and implanting with said second-type dopant at a higher concentration the buried layers to compensate for said first-type dopant.

17. An isolation trench structure, comprising:

a substrate having a buried layer and an epitaxial region formed therein;

a plurality of isolation wells formed in the substrate; and

a dielectrically insulated trench formed in intervening areas between each of the isolation wells and located at the edges of the isolation wells, each trench comprising a central contact region surrounded by insulating dielectric regions, each central contact region in contact with the buried layer.

18. The structure of claim 17 wherein the central contact region is formed of electrically conductive material.

19. The structure of claim 17 wherein the central contact region comprises doped polysilicon material.

20. An isolation trench structure formed in a semiconductor substrate having a buried region, comprising:

an isolation structure formed in the substrate to define a plurality of isolation wells, the isolation structure comprising a plurality of trenches, each trench having sidewalls lined with a insulating dielectric material to define a central cavity, and a conductive material filling the central cavity and in contact with one of either the substrate and the buried region to provide a conductive path to the substrate surface.

21. The process of claim 20, further comprising filling the trenches with a conductive material to form a plurality of contact regions to the buried layers of the device.

22. A process for fabricating an integrated device with an isolation structure, comprising:

providing a substrate doped with a first dopant type;

masking the substrate, implanting and diffusing dopant of a second type to form a buried layer;

growing an epitaxial region doped with the dopant of the second type;

oxidizing the epitaxial region and depositing a layer of silicon nitride;

depositing photoresist, exposing and developing the photoresist, sequentially etching the nitride and thermal oxide away from regions uncovered with the photoresist, and removing the photoresist to form trenches;

dry etching the silicon underneath as far down as the buried regions to pierce the bottoms of the trenches; and

oxidizing the trench sidewalls.

23. A process for fabricating an integrated device with an isolation structure, comprising:

providing a substrate doped with a first dopant type;

masking the substrate, implanting and diffusing dopant of a second type to form a buried layer;

growing an epitaxial region doped with the dopant of the second type;

forming a plurality of trenches;

depositing polysilicon material onto the entire surface of the substrate such that the surface is contacting the buried layers;

implanting the first-type dopant in the entire surface directly after depositing the polysilicon to lower the polysilicon resistivity and form resistive contacts; and

masking and implanting with the second-dopant at a higher concentration than the implanting and diffusing dopant step above in the buried layers to compensate for the first-type dopant.